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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,818	05/09/2001	Brian Sander	03942-237	5477

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EXAMINER	
DEPPE, BETSY LEE	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,818	SANDER, BRIAN	
	Examiner	Art Unit	
	Betsy L. Deppe	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2005* is/are: a)☒ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see last paragraph starting on page 8, page 10, lines 9-12, page 11, line 17 - page 12, filed January 31, 2005, with respect to the rejection(s)of claim(s) 1-9 under 35 USC 103(a) have been fully considered and are persuasive. Lee et al. in view of Dent does not disclose the sampling, performing and combining steps recited in claim 1 or the corresponding limitations recited in claim 5. Furthermore, Lee et al. in view of Dent does not teach the steps recited in claim 8 or the second logic section recited in claim 9. Therefore, the rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yamada et al. (US Patent No. 5,892,384), Staszewski et al. (US Patent No. 6,606,004 B2) and Sevenhans et al. (US Patent No. 5,528,637).

Drawings

2. The drawings were received on January 31, 2005. These drawings are accepted for the purposes of overcoming the objections raised in the Office Action mailed October 4, 2004.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the

description: 405.1-405.8 on page 4, line 23 - page 5, line 14. Figure 4 shows "5.1-5.8" while the detailed description uses reference signs "405.1-405.8."

4. Figure 4 is objected to because the "Alias" signal that is provided to Decision Logic should not be shown as an output of summation element 409 since summation element 409 does not generate this signal. It appears that Figure 5 more accurately depicts the "Alias" signal.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1 and 9 are objected to because of the following informalities:

in claim 1, line 11, it appears that "second intermediate values" should be "a second intermediate ***value***" since the transition detection for *each* delayed version of the derived clock signal produces a single value (see 407 and 405e in Figure 4); and

in claim 9, line 6, "values" should be "value". Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. With regard to claims 1-7, it is unclear what is meant by the limitation in claim 1, lines 4-6 and claim 5, lines 4-7 is confusing. For example, is the derived clock signal provided to the input of the first delay element in a series of delay elements to form the multiple delayed versions of the derived clock signal? Or is the derived clock signal provided simultaneously to multiple delay elements? What is meant by "each delayed version following a first delayed version in the sequence being more delayed than a previous delayed version in the sequence?"

9. With regard to claims 5-7, it is unclear whether "each" in claim 5, line 8 is referring to each of the sample chains or each of the logic elements.

10. With regard to claims 8 and 9, it is unclear how the formed "number stream" recited in the last line of the respective claims relates to the known and unknown clock signals in the preamble. According to the preamble, the number stream represents the frequency/phase of clock signals and one of the clock signals is a known clock signal while another clock signal is an unknown clock signal. So does the number stream represent the frequency/phase of the known clock signal or the unknown clock signal?

11. In claim 9, lines 7-9, it is unclear if the received alias value is used to form the number stream or if the number stream is based only on the combination of intermediate values.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1, 2 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al. (US Patent No. 5,892,384). Figure 2 of Yamada et al. discloses the claimed invention including circuitry for forming a derived clock signal ("waveform reform circuit" and 2), a delay chain of logic elements (3), multiple sampling chains (4), multiple transition detection circuits (5) and a combining circuit (6) that sums (i.e. "overlays" in column 14, lines 47-50). (See also column 14, lines 10-50)

14. Claims 8 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Staszewski et al. (US Patent No. 6,606,004 B2). (See Figure 15)

15. With regard to claim 8, Figure 15 of Staszewski et al. discloses applying to a digital circuit (i.e. the multiplexer) an alias value (i.e. the signal output from the sigma-delta modulated delay control) and forming a number stream (w_v) in accordance with the alias value).

16. With regard to claim 9, Figure 15 of Staszewski et al. discloses a first logic section that includes multiple chains of flip-flops and a second logic section (corresponding to the multiplexer, the sigma-delta modulated delay control and the flip-flop connected to the output of sigma-delta modulated delay control).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sevenhans et al. (US Patent No. 5,528,637). Figure 1 of Sevenhans et al. discloses the claimed invention including circuitry for forming a derived clock signal (TDL), a delay chain of logic elements (TDL), multiple sampling chains (SM), multiple transition detection circuits (C1-C4, L1-L4) and a combining circuit (SPC). (See column 4, line 3 - column 5, line 6) The TDL reads on both the circuitry for forming a derived clock signal and a delay chain of logic elements since the output of the first delay element qualifies as a "derived clock signal" and the successive delayed clock signals constitute

delayed versions of the "derived clock signal." (See column 4, lines 16-21) However, Sevenhans et al. does not disclose that the signal ID defining the sampling times for the sampling means SM is a clock signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the circuit disclosed by Sevenhans et al. use a clock signal as "ID" in order to synchronize a received clock with a local clock. Since a clock signal is similar to the ID signal (i.e. both signals have data level transitions - see Sevenhans et al., column 1, lines 4-10), the circuit functions identically regardless of whether the ID signal is a non-periodic data signal or a periodic clock signal.

Allowable Subject Matter

19. Claims 3, 4, 6 and 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Betsy L. Deppe whose telephone number is (571) 272-3054. The examiner can normally be reached on Monday, Wednesday and Thursday (8:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272 - 2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Betsy L. Deppe
Primary Examiner
Art Unit 2637